REMARKS

Claims 15-22 are pending. Claims 1-14 and 23-37 are cancelled and claims 38-43 are added.

Summary of Telephonic Interview

The undersigned wishes to thank Examiner Arcos and Supervising Examiner Bullock for taking the time to conduct a telephonic interview on January 23, 2008. During the interview, the undersigned proposed amending claims 15 and 16 to overcome the Section 112 rejections. Also, Examiner(s) suggested amending claim 15 to more clearly claim in the body of the claim that the Applicant's method occurs before the processing of the task begins to better distinguish over the MacDonald reference.

Claim Amendments

While the Applicants disagree with the basis for certain rejections made in the Official Action, claims 15 and 16 are nonetheless amended to expedite prosecution. Claims 38-43 are added. No new matter has been added due to these amendments and support for these amendments can be found throughout the Applicant's specification and figures.

Restriction Requirement

The Office asserts that a Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Group I, claims 1-14, drawn to a method of scheduling process classified in class 71 8, subclass 102.

II. Group II, claims 15-22, drawn to memory resource allocation, classified in class 71 8, subclass 104.

III. Group Ill, claims 23-32, drawn to CPU interrupts, classified in class 710, subclass 260+

IV. Group IV, claims 33-37, drawn to Graphic user interface, classified in class 71 5.

During a telephone conversation with Mr. Ari Gilder on 10/02/2007, a provisional election was made without traverse to prosecute the invention of group II, claims 15-22. Applicant in replying to this Office action must make affirmation of this election. Claims 1-14 and 23-37 are withdrawn from further consideration by the examiner, 37 CFR 1 .A 142(b), as being drawn to a non-elected invention.

Accordingly, the Applicants hereby elect group II, claims 15-22 without traverse and withdraw claims 1-14 and 23-37 from further consideration.

Claim Rejections under 35 U.S.C. §112

The Office has rejected claims 15-22 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicant regards as the invention. Specifically, the Office asserts that in claim 15 "it is unclear where the memory resources reside; it is not clearly understood whether they are in the coprocessor or different place," that "it is unclear what is considered proper location," and that "it is unclear how the processing is done." Additionally, with regards to claim 16, the Office asserts that "it is unclear what is GPU abbreviated from?"

The Applicants respectfully amend claims 15 and 16 to clarify where "memory resources" reside and what is meant by "processing said indicator" and "GPU." However, the Applicants assert that the meaning of "proper location" in line 5 of claim 15 is clear and definite. As support for this assertion the Applicants direct the attention of the Office to paragraph [0136] of the Applicant's specification which clearly describes what is meant by "proper location" and which recites:

> [0136] ***Note that during a context switch, a coprocessor can retranslate virtual address in use by the context being restored. This will ensure that memory resources are located in the proper place, instead of allowing the coprocessor to make a potentially false assumption that those addresses are referencing the same physical pages as before the context switch.*** Note also that in conjunction with various embodiments of the invention, it will be beneficial to allow multiple entries in a single page table or across multiple page tables to refer to the same physical pages.

Accordingly, the Applicants request that the Office respond favorably and withdraw these rejections.

Claim Rejections under 35 U.S.C. §103

Claims 15-18 and 22 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over U.S. Patent Number 5,247,674 to Masauki Kogure (hereinafter "Kogure"), and in view of US Patent Number 5,696,927 to MacDonald et al. (hereinafter "MacDonald"). Additionally, claims 19-21 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Kogure, in view of MacDonald, and in view of U.S. Patent Number 5,220,653 to Miro et al. (hereinafter "Miro").

In rejecting claim 15, the Office asserts that "MacDonald teaches preparing a task for processing in a coprocessor by paging memory resources (address) associated with the task into coprocessor readable memory (Col 3, lines 24-27)". The Applicants disagree and assert that at Col. 3, lines 24-27 MacDonald simply discloses an address mapping hierarchy which includes page tables entries mapped from a virtual address to physical memory. This is clear in the cited passage which recites,

> The ***address mapping hierarchy includes*** page tables having page table entries which map from a first portion of virtual addresses to respective pages in physical memory.

This is not the same or even similar to the Applicant's invention and nowhere in the cited passage does MacDonald teach, suggest or even mention "preparing a task for processing in a coprocessor" or "paging memory resources within the coprocessor associated with the task into coprocessor-readable memory."

Moreover, the Office asserts that MacDonald teaches "sampling the memory resources to determine if all required memory resources (reference page table) are in a proper location (corresponding page directory entry) in the coprocessor-readable memory." The Applicants disagree and assert that MacDonald does not teach this element. In making this assertion, the Applicants point out that they have found no such teaching in the disclosure of MacDonald and the Office has similarly pointed out no such teaching.

The Office further asserts that MacDonald teaches "recording whether all required memory resources are in a proper location in the coprocessor-readable memory (Col. 10, lines 13-19)," and "said recording generated an indicator memory resource that is associated with the task (Col. 10, lines 13-19), where page table availability in memory is an indicator as claimed." However, what MacDonald actually teaches is mapping the contents of the

reference page table entry to a physical memory page and if the page is not available generating a fault page. This is clear from the passage which recites in part,

> ...***the contents of the page table entry are used to map to a particular physical memory page*** in step 516. ***If the physical memory page so mapped is unavailable*** in memory, as indicated by a cleared state of the page present bit 403 in the corresponding page table entry (see decision point 518), ***then a page fault is triggered*** in step 519.

This is not the same or even similar to the Applicant's invention and nowhere in the cited passage does MacDonald teach, suggest or even mention "recording whether all required memory resources are in a proper location in the coprocessor-readable memory." In fact, MacDonald does not even disclose, teach or suggest checking to see if all required memory resources are in a proper location in the coprocessor-readable memory."

Additionally, the Office asserts that MacDonald teaches that "if said indicator resource indicates that all required memory resources are not in a proper location in the coprocessor-readable memory, the coprocessor stops processing the task (Col. 9, lines 63-67; col. 10, lines 1-2)." The Applicants disagree and assert that MacDonald actually discloses and teaches continuing processing the task and only disabling those portions not available. This is in direct contradiction to the Applicant's invention and clearly stated in the cited passage which recites,

> If the referenced page table is not present in memory (see decision point 512), a page fault is triggered in step 514, although as previously discussed, a preferable implementation of operating system component 292 ***would disable paging for those portions of memory containing the directories and tables of address mapping hierarchy 350 and compressed page mapping hierarchy 360***.

This is in contradiction with the Applicant's invention which stops processing the task completely. Accordingly, it is clear from the above discussion that neither Kogure or MacDonald disclose, teach or suggest the elements of Applicant's amended claim 15.

Furthermore, the invention in MacDonald is accomplished after the task has begun processing while the Applicant's invention occurs before the processing of the task begins. Accordingly, in light of the discussion hereinabove, it is clear that the Applicant's invention is completely different from the invention of MacDonald.

For the foregoing reasons, the Applicants respectfully submit that amended claim 15 is patentably non-obvious over Kogure and MacDonald. Inasmuch as claims 16-22 depend either directly or indirectly from amended claim 15, they too are patentably non-obvious over Kogure and MacDonald for the same reasons. Nevertheless, the Applicants wish to point out the following additional reasons why certain dependent claims are patentably non-obvious over Kogure and MacDonald.

Regarding claim 17, the Office asserts that "MacDonald teaches the task is represented by a DMA buffer" and directs the Applicant's attention to col. 7, lines 5-7 as support. However, the Applicants assert that MacDonald simply teaches that the contents are dynamic and is clearly indicated in the cited passage which recites,

> The contents of each hierarchy are dynamic with changes in the page-in/page-out status and with the compression status of given page.

This is clearly not the same as that claimed in Applicant's claim 17.

Regarding claim 18, the Office asserts that "MacDonald teaches that the coprocessor stops processing the task because processing said indicator memory resource generated a page fault" and directs the Applicant's attention to col. 9, lines 63-67; col. 10, lines 1-2 as support. However, as discussed hereinabove with regards to amended claim 15, MacDonald clearly does not teach stopping the processing of the task due to generation of a page fault. In fact, in direct contradiction to the Applicant's invention MacDonald teaches continuing the processing of the task and only disabling the affected portions of memory.

Regarding claims 19 and 20, the Office asserts that "MacDonald teaches that all required memory resources can be brought to a proper location in coprocessor-readable memory at a later time (Col. 10, lines 23-28)," that "Miro teaches maintaining a list of tasks that the coprocessor stopped processing (Col. 11, lines 1-4; 96, Figure 10)" and that "Miro teaches the later time is determined based on priority of tasks on the list of tasks (Col. 4, lines 1-3)." The Applicants disagree and as discussed hereinabove with regards to claim 15, MacDonald clearly does not teach or disclose that "all required memory resources can be brought to a proper location in coprocessor-readable memory at a later time." Additionally, element 96 in Figure 10 and the text at col. 11, lines 1-4 of Miro simply discloses a FIFO holding queue and clearly does not disclose or teach "maintaining a list of tasks that the

coprocessor stopped processing" and that "the later time is determined based on a priority of tasks on the list of tasks." In fact, Miro makes no mention of tasks (or a priority of tasks) that a coprocessor stopped processing. This is clearly not the same or even similar to that claimed by the Applicants.

Regarding claim 21, Miro does not disclose "a periodic priority boost that increases the priority of one or more tasks on the list of tasks to ensure that all tasks eventually can be processed" as asserted by the Office which directs the Applicant's attention to lines 12-18 of the Abstract of Miro as support. However, what Miro does disclose at the cited passage is simply prioritizing the holding queue. As discussed hereinabove with regards to claims 15 and 19, Miro does not disclose a list of tasks that the coprocessor stopped processing and thus, cannot disclose prioritizing these tasks.

In light of the discussion hereinabove, the Applicants assert that claims 15-22 are clearly patentably non-obvious over Kogure, MacDonald and Miro and are thus allowable.

CONCLUSION

For all the foregoing reasons, the Applicants respectfully submit that the present application is now in condition for allowance

Date: January 31, 2008

/Nathaniel Gilder/
Nathaniel Gilder
Registration No. 53,233

Woodcock Washburn LLP
Cira Centre
2929 Arch Street, 12th Floor
Philadelphia, PA 19104-2891
Telephone: (215) 568-3100
Facsimile: (215) 568-3439